

# Shiver Me Timers! Using Spread Spectrum Clock Generators

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Most methods used for EMI suppression have hardly changed in the last quarter century. The standard tool kit has largely consisted of components that filter and shield, and methods for improving layout. While these tools have become refined over time, nothing much in the kit would have seemed alien to an RF designer of a generation ago.

It was only in the last decade or so that a truly new approach was proposed, the spread spectrum clock generator (SSCG). It reduces EMI by modulating the clock frequency, thereby spreading radiated energy over a frequency range wider than the bandwidth of the standard receiver used to measure emissions. At any one frequency, the detected emission falls.

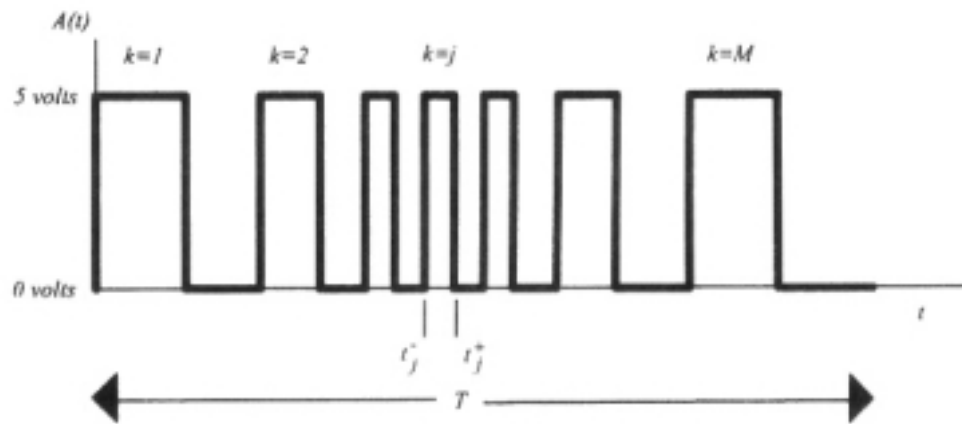
Spread spectrum techniques are hardly new. The tale of their invention is oft-told, and usually begins with the filing of a 1942 patent by George Antheil and the actress Hedy Lamarr. The patent disclosed a method of frequency hopping used to immunize radio controlled torpedoes from jamming. In the last two decades, the technique has become a fixture in the communications industry because of its advantages in range, immunity and security.

The use of spread spectrum clock generation to reduce emissions in digital devices was first proposed in a paper presented at the 10th Annual Power Electronics Seminar at the Virginia Power Electronics Center in 1992 (Ref. 1). Author Lin described the modification of a switching power supply circuit so as to modulate its switching frequency, thereby smearing its emissions over a broad swath of the spectrum. In the particular application described, a power supply's nominal switching frequency of 90 kHz was frequency modulated with a sine wave producing a frequency variation off +/- 15 kHz at a rate of 400 Hz. Substantial reductions in emissions resulted.

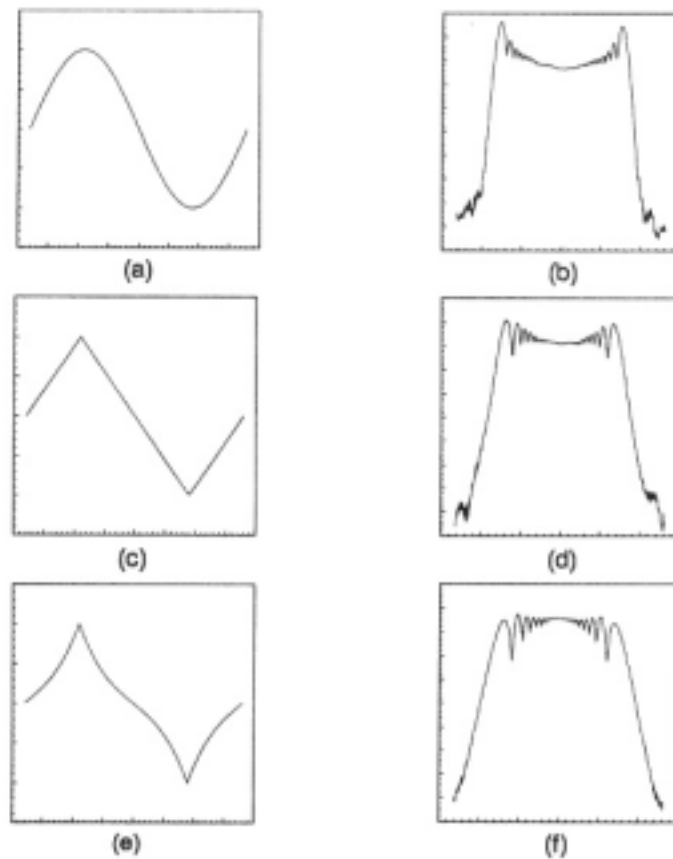
At the 1994 IEEE International Symposium on Electromagnetic Compatibility, authors Keith Hardin, John Fessler, and Donald Bush presented the results of their work to develop practical spread spectrum clock generator for use as a CPU clock in digital devices. The wide modulation frequency proposed by Lin was impractical for use as a clock generator. The authors proposed to vary the frequency of the clock only slightly, deviating a 20 MHz clock by +/- 125 kHz, a variation of only .625%. This resulted in a measured attenuation at the third harmonic, 60 MHz, of only 2 dB. However, as the harmonic number increased so did the attenuation. At the 20th harmonic, 400 MHz, the measured attenuation was 10 dB.

Lexmark International (formerly IBM's Office Products Division) had sponsored this research. Early on, it was observed that the sinusoidal waveform used by Lin to frequency modulate the clock in his power supply did not produce optimal EMI suppression. As shown in Figure 2, the

frequency distribution resulting from the FM modulation of an oscillator via a sine wave produces a spectrum that is peaked at its extremities. The reason for this has to do with the rate of change (derivative) of the sine wave. Its rate of change slows as the sine wave reaches its peak values. As shown in Figure 2(b), this happens at the ends of the spectra generated, and it is there that the oscillator “hangs out” a little longer than it does elsewhere. Better results were achieved when a triangular wave was used to modulate the clock as shown in Figures 2(c) and 2(d). But the engineers at Lexmark found that an optimal waveform was the one shown in Figure 2(e). This produced relatively flat spectra across the deviated range. The waveform of Figure 2(e), shown in greater detail in Figure 4, has become known as the “Lexmark Shape.” Lexmark received a patent on their design.



**Figure 1: A spread spectrum clock generator works by changing the period of the clock. In this illustration, the effect is exaggerated. From Ref. 2.**



**Figure 2: Different modulating profiles (on the left) produce different frequency spreading effects (on the right). The optimum profile is the one which produces the most even frequency distribution. This is produced using the modified triangle wave at 2(e) which has become known as the “Lexmark Shape.” From Ref. 2.**

The 1994 paper was greeted with a mixture of accolades and criticism. “This is like getting rid of a cow pie by stomping on it,” one critic said. No one questioned that the effect was real. However, critics argued that spreading the energy does not reduce it. Receivers that used bandwidths wider than 120 kHz, including televisions, could be adversely affected, they argued. The FCC rules, intended to protect a wide variety of devices but written long before the advent of spread spectrum devices only specified a 120 kHz measurement bandwidth.

Hardin, Fessler and Bush conducted a detailed study of the effects of spread spectrum clock generation on television reception. They concluded that most televisions are, more or less, indifferent to the interference caused by either a narrow band or a spread spectrum generated clock (Ref. 6). To avoid interference with the audio portion of a transmitted television signal, the authors did point out that the modulation frequency used should be greater than 20 kHz.

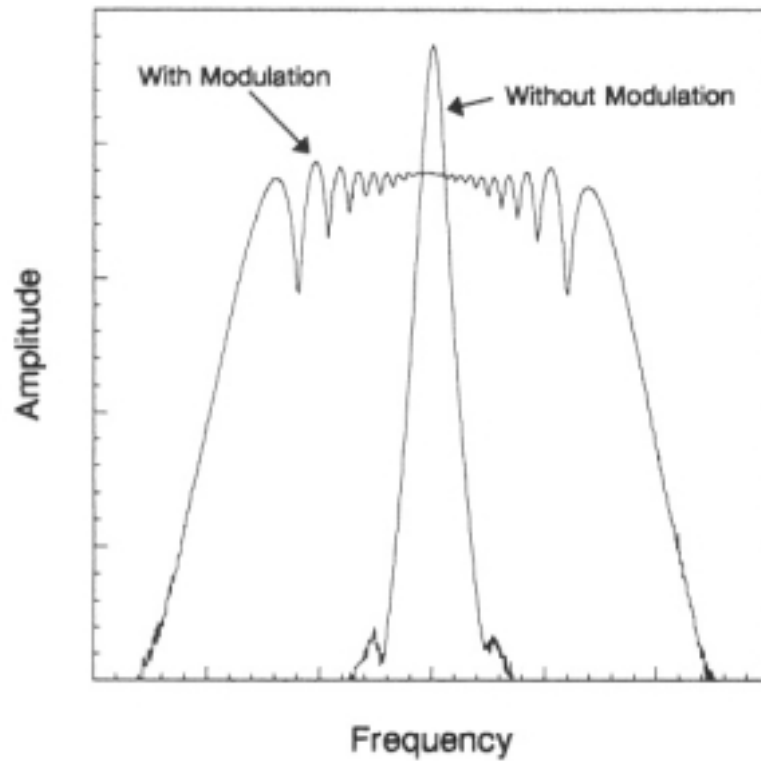


Figure 3: The frequency modulation produced by a SSCG reduces emissions, especially at the higher harmonics of the clock. From Ref. 2.

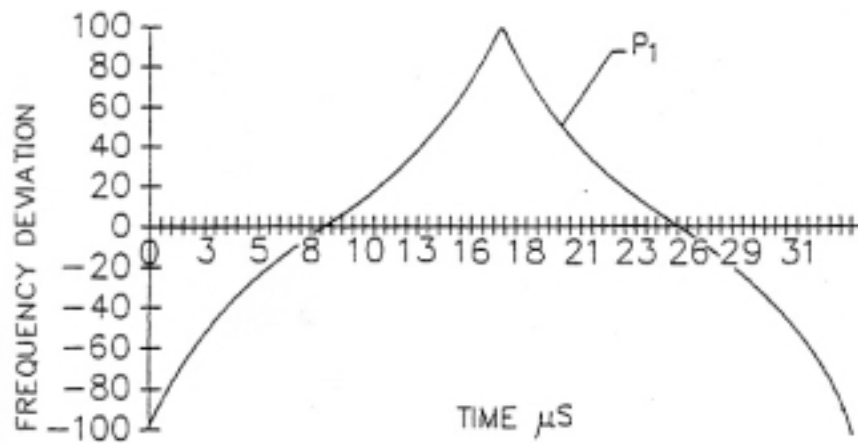


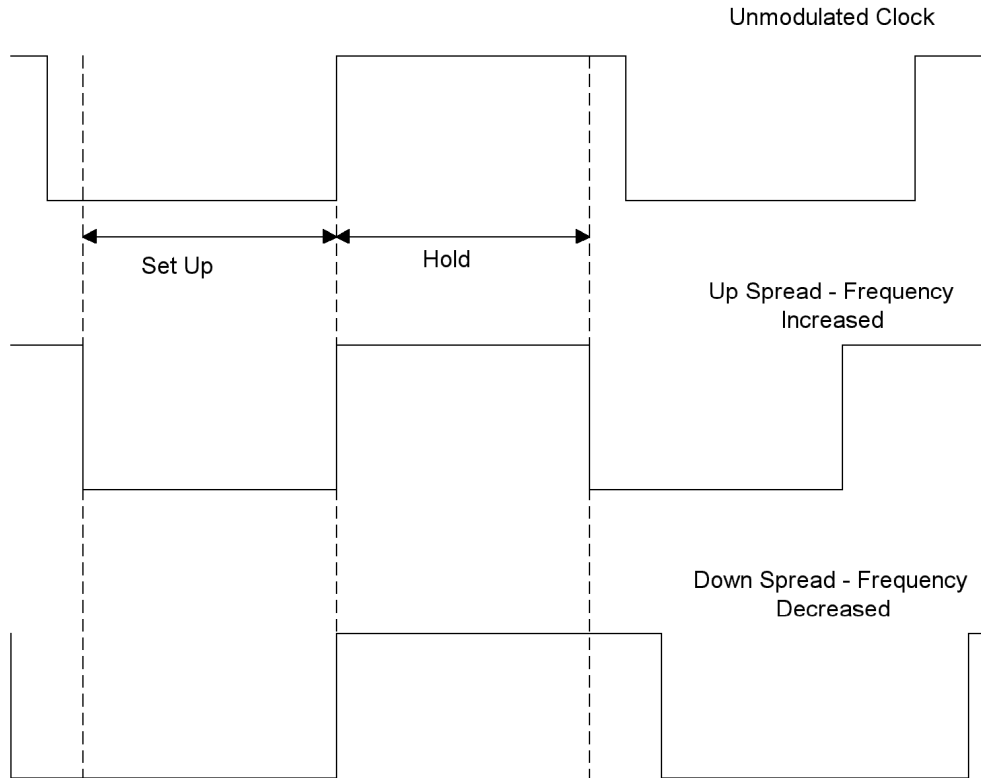
Figure 4: A close look at the “Lexmark Shape.” From Ref. 3.

But spread spectrum clocking is not without some inherent problems. For example, its use can create significant timing issues. Certain applications simply cannot tolerate a wandering clock.

Video displays, for example, may shiver noticeably. Many forms of communications require a synchronous clock in line with tight specifications. According to Dr. Howard Johnson, the author of *High Speed Digital Design: A Handbook of Black Magic*, (Prentice Hall, 1993), the technique should not be used for timing on Ethernet, Fiber Channel, FDDI, ATM, SONET or ADSL applications. Unless the clock is pristine, these applications can suffer from poor locking, failure to lock or data errors.

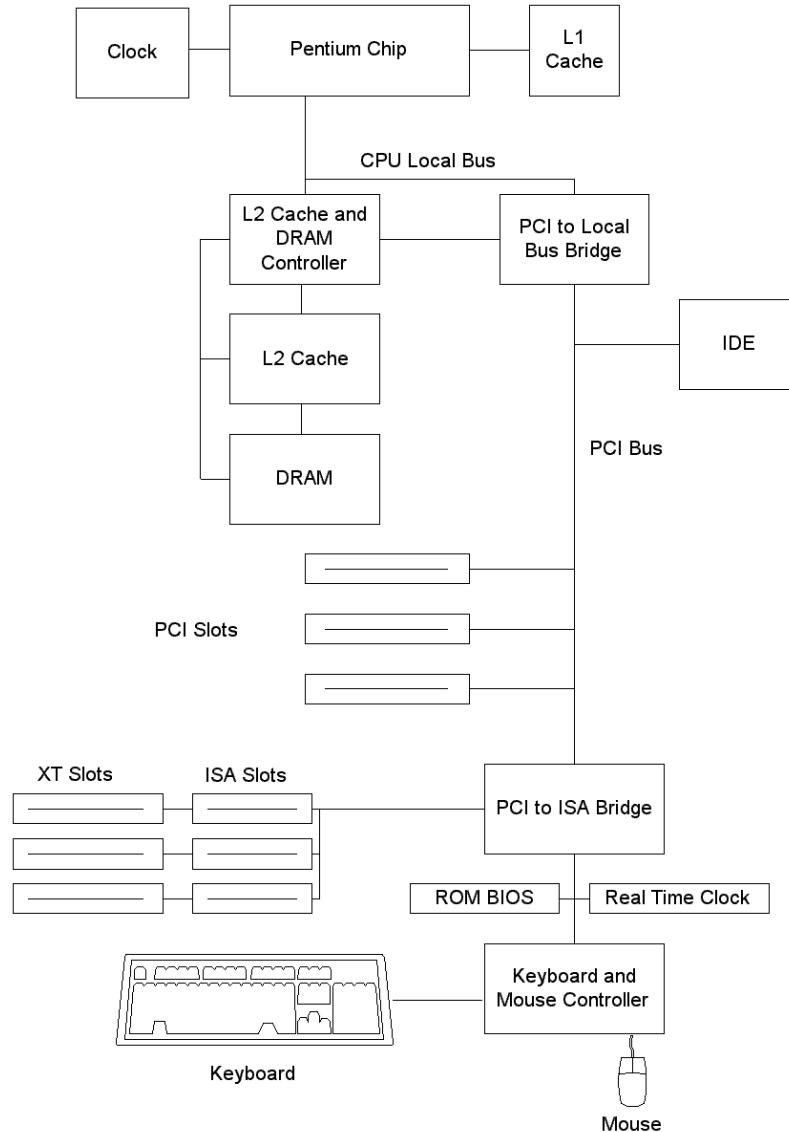
In order to evaluate the suitability of a spread spectrum generated clock in your design, three timing specifications should be reviewed: peak-to-peak jitter, cycle-to-cycle jitter and setup/hold times. Peak to peak jitter is defined as the total percentage of spreading divided by the center frequency, and is usually specified in nanoseconds. For example, a 50 MHz clock undergoing a spread of +/- .625 percent (1.25 percent in total) would produce a peak-to-peak variation of .25 nanoseconds (20 nanoseconds times 1.25 percent). Cycle-to-cycle jitter is the amount of variation in picoseconds per cycle and depends on the wave shape and frequency used for modulation. If, in our example a 50 kHz triangular wave was used, the cycle-to-cycle jitter would be calculated as follows. The +/- .625 percent frequency change would occur over one-half cycle of the triangular wave, or 10 microseconds. Ten microseconds corresponds to 500 cycles of the 50 MHz clock. Since the peak-to-peak variation was .25 nanoseconds, the cycle-to-cycle variation is .25 nanoseconds divided by 500, or .5 picoseconds.

In most applications, neither the peak-to-peak jitter nor the cycle-to-cycle jitter of a SSCG is of significant concern. That is not true, however, for set up and hold times illustrated in Figure 5. As the frequency is increased, set up and hold margins decrease. Some devices use such tight set up and hold margins that any frequency increase cannot be tolerated. For that reason, spread spectrum clock generation is sometimes implemented using a “down spreading” only approach. Instead of shifting the clock frequency above or below the carrier, the frequency is only shifted downward, which should only increase the setup and hold margins.



**Figure 5: Set up and hold times must be considered when the clock speed is changed. The use of “down spreading” can help to avoid problems caused by increasing clock speeds.**

Spread spectrum clock generators can be used in Pentium machines, but with care (Figure 6). In the example below, a clock generator runs at 66.6 MHz. Internally, a phase lock loop arrangement is used to multiply this clocking frequency by a factor of 5, producing an internal CPU clock of 400 MHz. This multiplied clock is used to drive machine cycles internally and to communicate with the Level 1 cache. Communication with DRAM memory and with the Level 2 cache is through an external local bus. A local bus to PCI bridge drives the PCI bus which in our example utilizes a 33.3 MHz clock. A further bridge connects the PCI bus through to the ISA slots, XT slots, and mouse and keyboard controllers.



**Figure 6: A typical Pentium system.**

It is the internal CPU bus, local bus and PCI bus which typically give rise to most of our emissions problems and therefore are the target of most spread spectrum designs. Figure 7 contains the specifications for the IC Works W48C101-01 Spread Spectrum Clock Generator. Input pins can be used to select the CPU clock speeds and whether a center or down spreading type frequency modulation is to be used. Note that both the CPU clock and the PCI clocks are modulated. A second, independent clock system generates a 48 MHz clock for the universal serial bus, and that clock is not modulated.

## Spread Spectrum BX System Frequency Generator

### Features

- Maximized EMI suppression using IC WORKS' spread spectrum technology
- Four copies of CPU output
- Eight copies of PCI output (Synchronous w/CPU output)
- Two copies of 14.318MHz IOAPIC output
- Two copies of 48MHz USB output
- Three buffered copies of 14.318MHz reference input
- Input is a 14.318MHz XTAL or reference signal
- Selectable 100MHz or 98MHz CPU outputs
- Power management control input pins

### Key Specifications

Supply Voltages:

VDDQ3 = 3.3V±5%  
VDDQ2 = 2.5V±5%

CPU0:3 Jitter (Cycle to Cycle): 200ps  
CPU0:3 Output Skew: 175ps  
PCI\_F, PCI1:7 Output Skew: 500ps  
CPU to PCI Output Skew: 1.5 - 4.0 ns (CPU Leads)

Test mode and output tristate

Logic inputs have 200K ohm pull-up resistor except SEL100/98#

Figure 1 Block Diagram

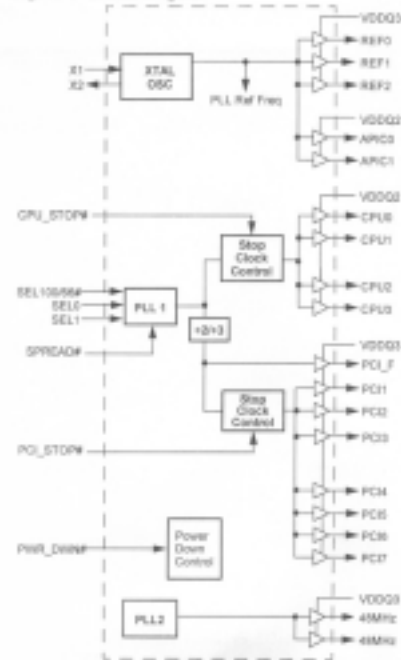


Table 1 Pin Selectable Frequency (Note)

SEL100/98#	SEL1	SEL0	CPU (MHz)	PCI (MHz)	SPREAD#
0	0	0	10-Z	10-Z	Don't Care
0	0	1	66.6	33.3	±0.9% Center
0	1	0	66.6	33.3	-1% Down
0	1	1	66.6	33.3	-0.9% Down
1	0	0	X10	X1/6	Don't Care
1	0	1	100	33.3	±0.9% Center
1	1	0	100	33.3	-1% Down
1	1	1	100	33.3	-0.9% Down

Figure 2 Pin Diagram



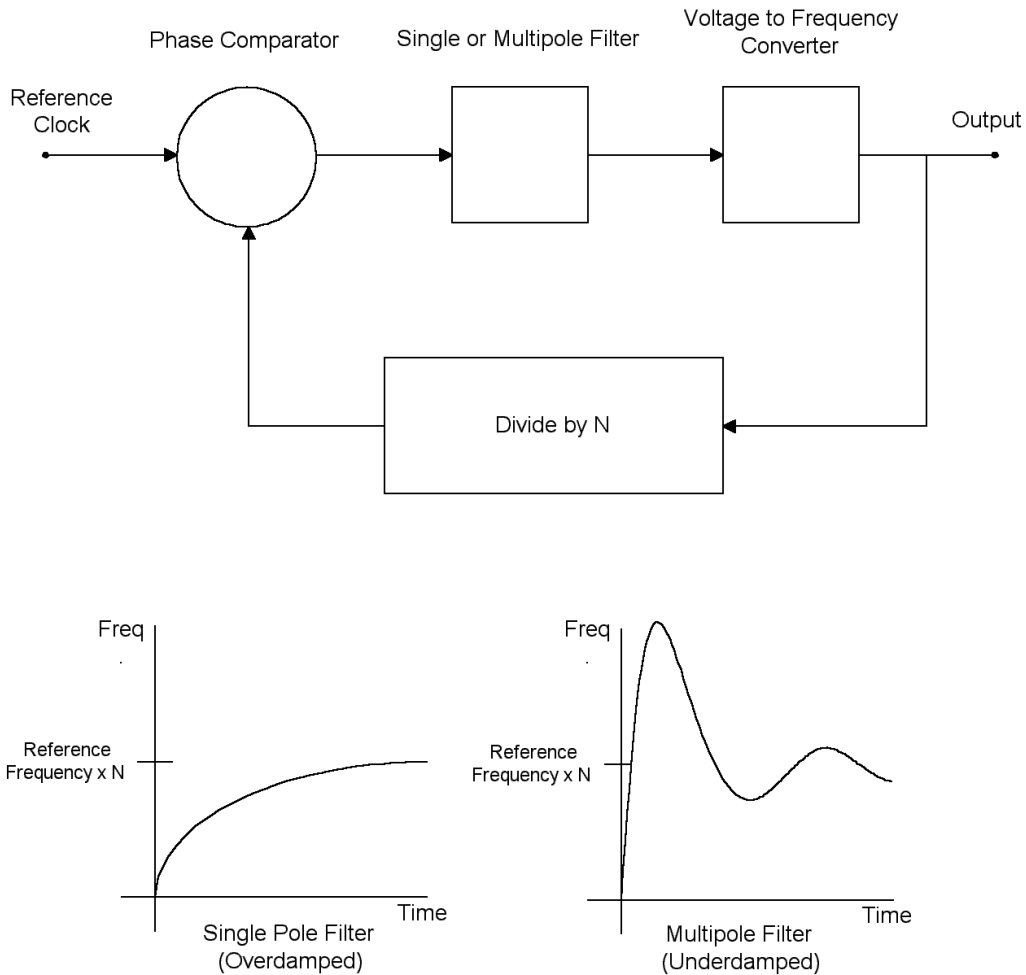
Table 2 Order Information

Part Number	Freq. Mask Code	Package
W48C101	-01	H = SSOP (300 mil)

Figure 7: The specification for a SSCG used with Pentium machines.

Techniques such as down spreading can resolve most timing concerns, but preserving the Lexmark shape is harder than it at first might seem. The reason for this is the internal multiplication that is used to increase clock speed. As mentioned, this internal multiplication is done by way of a phase lock loop (PLL). A PLL uses a feedback system to compare a frequency-divided version of the output signal to the input signal, thereby locking the two in frequency (Figure 8). Like most feedback systems, however, an instantaneous change at the input does not result in an instantaneous proportional change at the output. Rather, the output can approach its final value asymptotically (as in a single pole, "over damped" feedback system) or bounce around its final value (as in the case of a multiple order, "under damped" system). Most phase

locked loops used for frequency multiplication in CPUs are third order, making predictions as to how the output frequency will change with changes to the input difficult to predict (Reference 10).

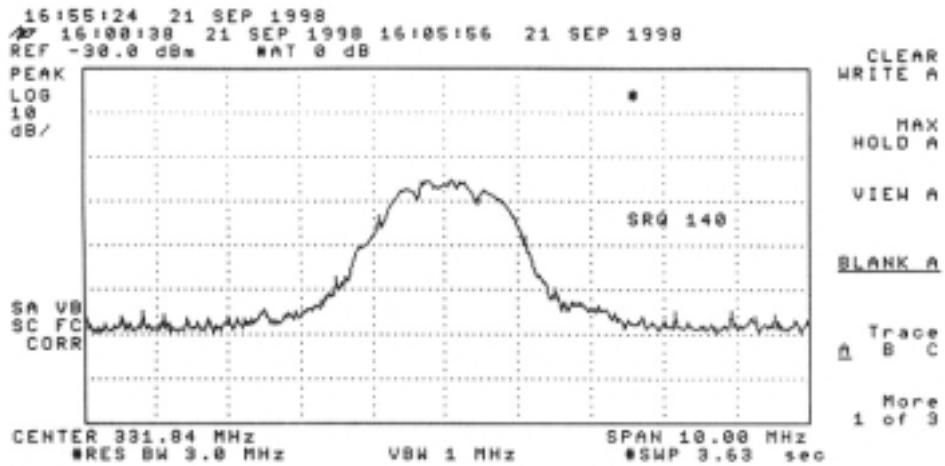


**Figure 8: A phase locked loop multiplies the input frequency by dividing the output frequency and feeding back the divided signal to the input, where it is compared to the input reference clock. The response of the system to changes can be over-damped or under-damped.**

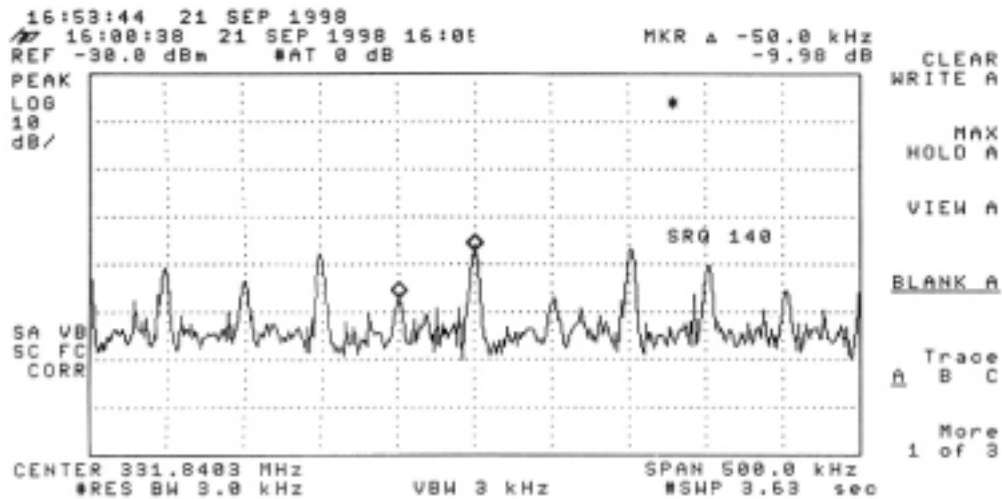
Remember that the Lexmark work was focused on devising a carefully shaped, optimal “Lexmark” frequency spread. But when a PLL is in use, the resulting CPU frequency spread is unlikely to track this carefully crafted input. For this reason, use of an SSCG with any processor employing PLL multiplication requires careful consultation with the SSCG clock manufacturer and the manufacturer of the microprocessor. See the box for information on how to contact Intel and several of the SSCG manufacturers.

PC manufacturers now use SSCGs as a matter of course. For example, we used a near field probe to sample radiation from a Dell computer equipped with a Celeron processor. At a wide receiving bandwidth (IF bandwidth of 3 MHz, video bandwidth of 1 MHz) we could observe

SSCG operation in a down spreading mode. The percentage of modulation appeared to be on the order of .5%. Narrowing the bandwidth to 3 kHz allowed us to examine the modulation products. We found these spaced 50 kHz apart, indicating a modulation frequency of 50 kHz.



**Figure 9:** Our Dell Celeron machine apparently uses a spread spectrum clock in a down spread mode. Note the bandwidth used for the measurement: 3 MHz IF, 1 MHz video. Center frequency is 333 MHz.



**Figure 10:** At a narrower bandwidth, 3 kHz, individual modulation products were resolved. It appears that a 50 kHz modulation frequency was in use.

Despite some difficulties inherent in its use, spread spectrum clock generators are here to stay. You won't be able to use them for some communication designs, nor for video clock generators. Spread spectrum clock generation is better done in the down spreading mode where setup and hold time margins are less likely to be affected, if you can afford the slight decrease in speed. Manufacturers seem to be settling on spreads between .5% and 1% with modulation frequencies between 30 and 50 kHz.

## **Where to Look for More Information on Spread Spectrum Clock Generators:**

These **SSCG manufacturers** have set up web sites:

**Cypress Semiconductor** - <http://www.cypress.com/>

**Integrated Circuit Systems** - <http://www.icst.com/>

**NEL Frequency Controls, Inc.** - <http://nelfc.com/>

**Lexmark International** has set up a website which also contains information on SSCGs:  
<http://www.lexmark.com/sscg>.

**Intel** has also set up its own site for developers: <http://www.intel.com/design/>

## References:

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