

On-Chip Design For Better Noise Control

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ICs Can Be Designed To Minimize Emissions At The Source.

ICs can be designed to produce fewer emissions without compromising performance. In fact, good on-chip EMC design can go a long way towards eliminating other undesirable noise related problems, such as “ground bounce.” And we are not talking about frequency-modulated clocks here. What we are talking about are techniques that work to lower emissions without changing the clock frequency.

Before discussing how these techniques work however, we should review two main causes of unwanted emissions from digital designs. The first is illustrated in Figure 1. Here a clock driver is shown driving a distant load. The clock driver, like all integrated circuits, has certain internal characteristics including its internal inductance (L_0) and output resistance (R_0) that affect its performance. In application, a designer may add a series resistance (R_S), usually to match trace impedances. Other impedances present in a circuit will be the impedance of the load (Z_2), the trace impedance Z_1 and the impedance of the return plane, Z_3 .

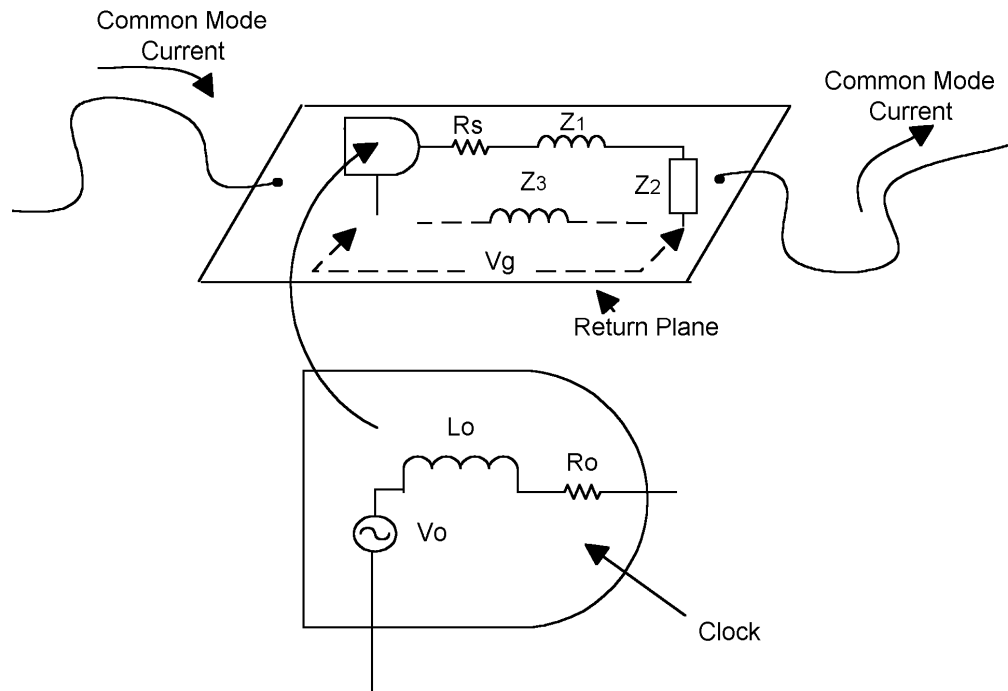


Figure 1: A voltage V_g causes wires attached to the return plane, directly or incrementally, to radiate as if they were antennas. The voltage V_g is a product principally of the clock's high frequency currents and the return plane's impedance Z_3 .

Impedance Z_3 is the principal culprit we are concerned with. Return currents create a voltage drop, V_g , across Z_3 . This voltage drives any wires that are attached to the return plane (directly or incrementally) as if they were antennas. The result can be a surprising amount of radiation for even the simplest of circuits.

Even solid ground planes exhibit some inductance per unit length owing to their finite size. The reason for this is a phenomenon known as “lost flux.” Some of the flux generated by the wire connecting the clock in Figure 1 to the load Z_2 does not circulate around the wire itself. Some curves around the return plane owing to its finite size, and it is this “lost flux” which creates (and can be used to calculate) Z_3 . The more flux that is “lost” in this way, the greater Z_3 .

The greater the return current, the greater the voltage drop across Z_3 . Some designers have sought to lower the return current by raising R_S . There is a practical limit, however. Raising the sum of R_0 and R_S to more than 60-100 ohms can degrade rise times. In any event, most designers prefer to match R_S to the impedance of the transmission line formed by the wire and the plane in order to reduce reflections.

Reducing or increasing the rise time of the clock will increase or reduce, as the case may be, the voltage drop across Z_3 . Though an upper limit for the rise time is set by specification (two nanoseconds for AC logic, for example) clock drivers often operate much faster than that. The reason for this is that the two nanosecond rise time specified for AC occurs under full fan out. When not driving a full load, the output rise times are typically much faster -- on the hundreds of picoseconds for AC clock drivers.

A second cause of noise related problems is internal to the ICs themselves and is related to a specification known variously as I_{dd} Noise, I_{dd} Delta or “shoot through current.” Figure 2 illustrates how I_{dd} Delta is created. Two FETs form a basic inverting gate. When the input voltage is high, the P channel FET is off and the N channel FET on. Any load connected to the output is pulled down to the return. When the input voltage is low, the opposite occurs, and the output is pulled up to V_{cc} . When the output is pinned to either the return or V_{cc} very little current flows through the series combination formed by the P and N channel FETs. That is not true, however, during the transition between states. For a time during the transition, both the P and N channel FETs will be on, essentially creating a short across the supply. This brief burst of current is illustrated in Figure 3. The current peaks when the input is half way between the V_{cc} and the return. This peak is approximately 1 milliamp for high speed CMOS (HC) and about 4 mA for advanced CMOS (AC). (For 4000 or 74 C series logic it is insignificant.) Unfortunately, I_{dd} Delta is rarely shown on manufacturers’ data sheets and is highly variable, depending on process, temperature and supply voltage.

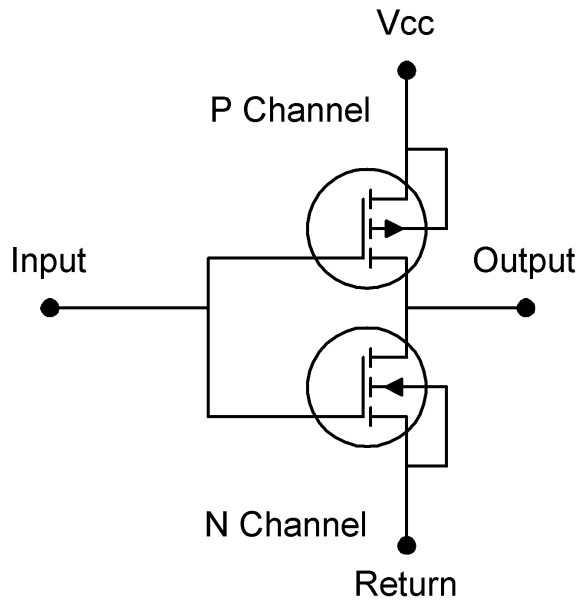


Figure 2: I_{dd} Delta is caused by the internal workings of integrated circuits. As the input transits from low to high or vice versa, a brief burst of current flows from V_{cc} to the return.

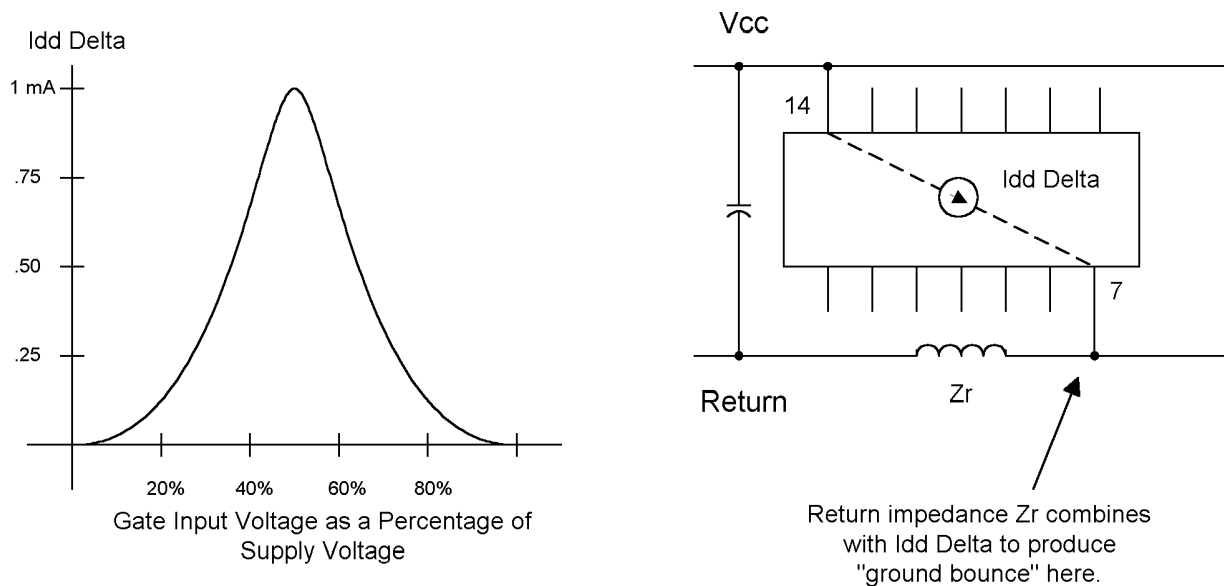


Figure 3: As the input voltage to the inverter in Figure 2 rises, I_{dd} Delta increases to a maximum in the middle of the transition range where both the P and N channel FETs are on. I_{dd} Delta can combine with any return impedance (Z_r in the figure) to produce ground bounce.

To minimize ground bounce and EMI, chip designers can try to achieve these two effects. First, the rise time of an output should not vary significantly with the capacitance of the load. That will

avoid cases where a lightly loaded AC driver, for example, could exhibit a rise time of a few hundred picoseconds. Second, designers could seek to reduce or eliminate I_{dd} Delta. To do that, they have to keep the driver's N and P channel FETs from turning on at the same time.

There have been many schemes proposed for achieving these objectives but few more widely cited than those invented by Jeffrey Davis of National Semiconductor Corporation in 1990. Davis' basic invention (Reference 1) is illustrated in Figure 4. The design is a tri-state inverter with a few extras. Here's how it works.

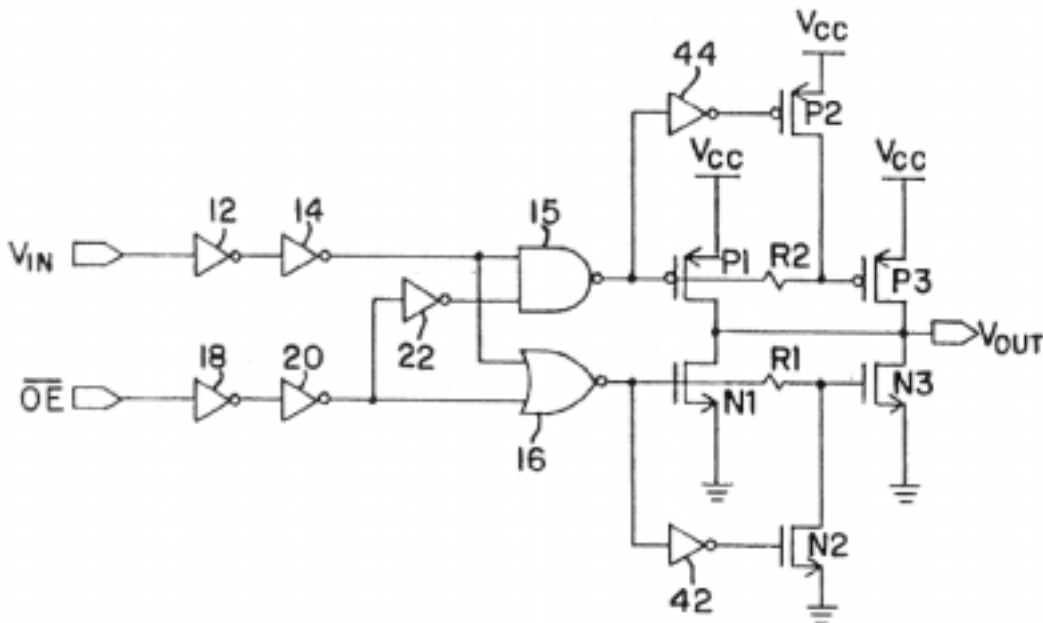


Figure 4: Davis' design is the most widely cited method for controlling emissions and ground bounce through integrated circuit design. It aims to control the output rise time and cut I_{dd} Delta.

We will assume that the output enable, OE, is low, enabling the circuit to function. When V_{IN} is high, so is the output of inverter 14. The output of NAND 15 gate is low, which turns on the PMOS FET P1. The gate of P1 is connected to resistor R2, which is, in turn, connected to the gate of PMOS FET P3. In part because of the gate capacitances, P3 turns on a little bit slower than P1. This delay is significant, as we will explain shortly.

Also when V_{IN} goes high, the output of gate 16 goes low, turning off N1 and turning on N2. FET N2 robs voltage from the gate of N3 turning it off rather quickly (and much faster than if we waited for the N3's gate voltage to be drained through R1).

The parallel arrangements of P1/N1 and P3/N3 are the secrets to the design. P1 and N1 are geometrically small FETs. They have a relatively high ON resistance. They are used to charge and discharge low capacitance loads, on the order of a few tens of picofarads. For larger loads, muscle needed comes from the much larger FETs, P3 and N3.

This two-stage design tends to regulate the output rise time over a range of capacitive loads. When the capacitive load is small, it is P1 and N1 that do the driving. Their output resistance is relatively high and that combined with the trace and load capacitance dictates the output's rise time. By the time FETs P3 and N3 switch state, the action is effectively over. The output capacitance is charged, and little or no current flows from the load through those devices. If the capacitance loading the output is large, P1/N1 will have lesser effect, but will still have some, partially charging the output prior to N3 or P3 turning on. The two-stage combination of N1/P1 and N3/P3 helps stabilize the device's rise time over a wide range of loads. If better control is desired, the trick can be repeated a number of times with successive stages.

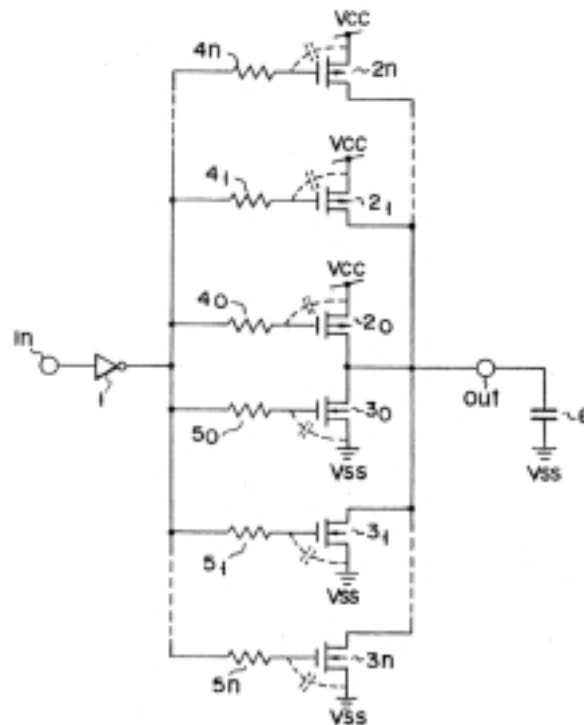


Figure 5: Other inventors have sought to build on Davis' work. This design uses multiple stages to better control rise times. (From Tanaka et al, US Patent No. 5,128,567.)

The Davis design also helps minimize I_{dd} Delta. Note that FETs N2/P2 will turn off N3/P3 quickly, and well before the opposing FET has time to turn on. That minimizes the currents from V_{CC} to the return (Figure 4). FETs P1/N1 will contribute some I_{dd} Delta. However those devices are small and will have relatively high on state resistances and therefore the I_{dd} Delta produced should be small. The Davis design achieves the twin benefits of controlled rise time and reduced I_{dd} Delta with a minimum of extra elements and additional propagation delay.

References

1. Davis, Jeffrey B., Patent No. 4,961,010 (1990).

2. Davis, Jeffrey B., Patent No. 5,036,222 (1991).
3. Davis, Jeffrey B., Patent No. 5,081,374 (1992).
4. G. Staas and N. Thompson, "The New Microcontrollers: Low EMI/RFI and Protection Features Provide Flexibility and Reliable Design," *Compliance Engineering*, March/April 1995, page 39.